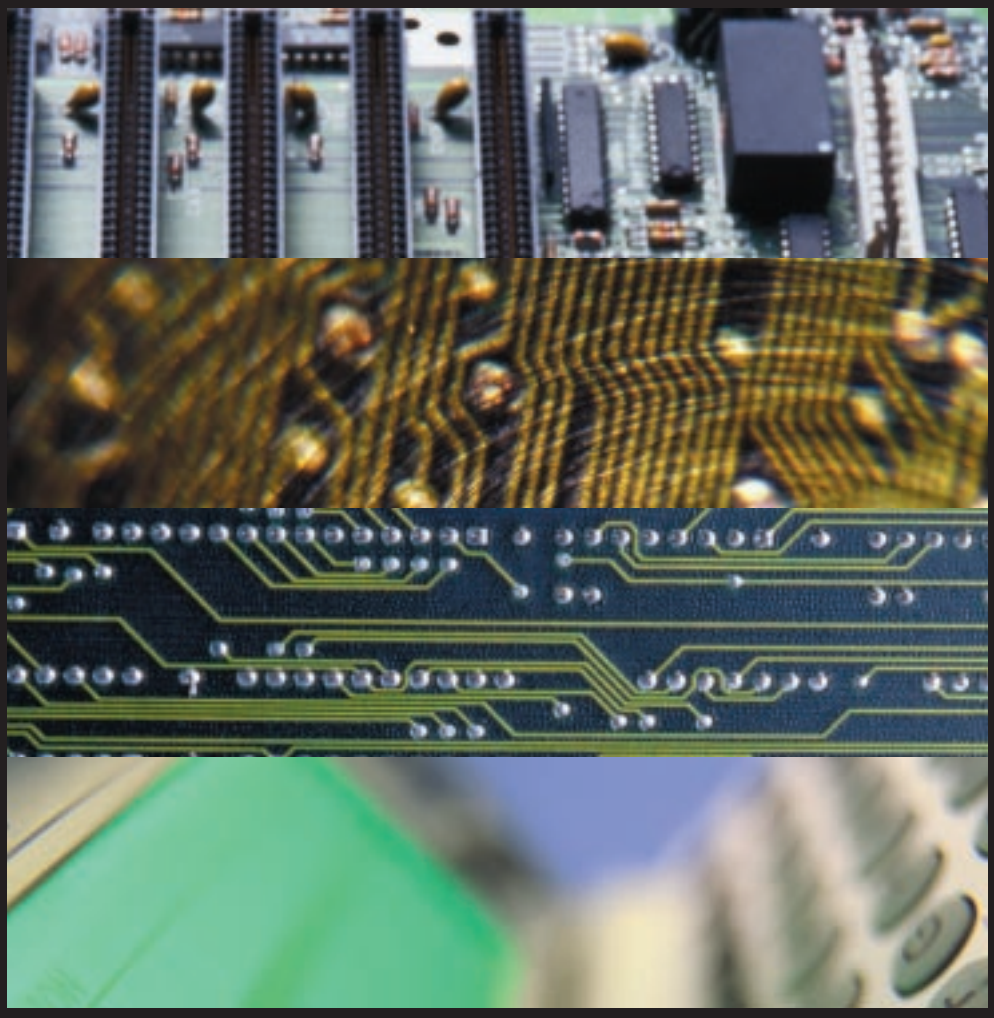
VANGUARD SERIES



IEEE ELECTRON DEVICES SOCIETY
INDEPENDENT SHORT COURSES

April 12, 2001- Santa Clara Marriott, CA
April 26, 2001- National Chiao Tung University, Taiwan

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INDEPENDENT SHORT COURSES

ULTRA-THIN GATE OXIDE AND HIGH-K DIELECTRICS

Professor JACK C. LEE
Cullen Trust for Higher Education Endowed Professorship in Engineering Department of Electrical and Computer Engineering
The University of Texas at Austin

April 12, 2001, Santa Clara (CA) Marriott

April 26, 2001, National Chiao Tung University Taiwan

TOPICS (tentative)

- Physical and chemical properties of SiO2 and Si/SiO2 interface
- Oxide characterization and testing methods
- Pre-oxidation cleaning
- Oxide reliability including breakdown mechanism and lifetime extrapolation
- Oxynitride gate dielectrics
- Effects of process-induced damages (e.g., plasma process)
- High-K gate dielectrics - potential candidates and technology
- Gate electrodes (e.g., polysilicon, metal) and their effects on gate dielectrics

COURSE OBJECTIVES

- Provide fundamentals of gate oxides and silicon interface
- Provide overview of gate oxide processes, surface preparation, reliability testing, breakdown mechanism and lifetime extrapolation
- Discuss the effects of post-oxide process damages (e.g., plasma damages)
- Discuss the gate electrode processes and effects on gate dielectrics
- Provide the status of high-K gate dielectrics

COURSE DESCRIPTION

The course will provide a detailed discussion of the current and future gate dielectrics. First discussed will be the fundamentals of SiO2 and Si/SiO2 interface, followed by an overview of oxide characterization techniques, reliability and lifetime extrapolation, and process-induced damages. Also discussed will be alternative gate oxide processes, including oxynitrides and high-K gate dielectrics.

WHO SHOULD ATTEND?

The IEEE EDS independent short courses are intended for experienced electrical and electronic engineers who need quick, intense information on the latest technologies, and who already have a practical understanding of their field.

The gate dielectrics course is especially intended for

- Gate stack engineers
- Process integration engineers
- Test and characterization engineers
- Yield enhancement and quality-control engineers

ABOUT THE INSTRUCTOR

DR. JACK C. LEE is Professor in the Electrical and Computer Engineering Department and holds the Cullen Trust For Higher Education Endowed Professorship in Engineering at The University of Texas at Austin. He received his B.S. and M.S. degrees in Electrical Engineering from the University of California at Los Angeles in 1980 and 1981, respectively; and his Ph.D. in electrical engineering from the University of California at Berkeley in 1988.

From 1981 to 1984, he was a Member of Technical Staff at the TRW Microelectronics Center, CA, in the High-Speed Bipolar Device Program, where he worked on bipolar circuit design, fabrication and testing. In 1988, he joined the faculty of The University of Texas at Austin. His current research interests include thin dielectric breakdown and reliability, high-K gate dielectrics and gate electrode, high-K thin films for semiconductor memory applications, electronic materials, and semiconductor device fabrication processes, characterization and modeling.

He has published over 200 journal publications and conference proceedings. Lee has been awarded two Best Paper Awards, numerous teaching awards and several patents. He has been invited to present his high-K gate dielectric work in numerous conferences, including the SRC Topic Research Conference on Reliability in Palo Alto, CA (Oct. 2000), the ULIS Workshop in Grenoble, France (Jan. 2001), the 6th Workshop on Formation, Characterization and Reliability of Ultra-thin Oxide in Japan (Jan. 2001), and as a keynote speaker at the Nano-Device Technology Symposium in Taiwan (April 2001).

THE VANGUARD SERIES

Through the Electron Devices Society (EDS), the Institute of Electrical and Electronics Engineers presents a new series of continuing education courses. The new IEEE EDS Vanguard Series is for the experienced engineer who is seeking in-depth information on advanced technologies that complements his or her own knowledge and practice. The modestly priced, one-day courses on leading edge technologies are taught by renowned experts in their fields. The courses are intended to serve the IEEE community as well as those with interest in advanced technology subjects related to devices and circuits.

SCHEDULE

Registration 8:00	Lunch (provided) 12:00
Class 8:30	Class 1:00
Break 10:30	Break 3:00
Class 11:00	Class 3:30 - 4:30

Certificates of completion will be awarded at the end of class.

For more information, please contact Vanguard Short Courses Manager Emily Sopensky at 877 566 4333 in the U.S. or email her at e.sopensky@ieee.org. See also www.ieee.org/eds/shortcourses/

For short courses delivered in **Taiwan,** see Prof. Steve S. Chung, Department of Electronics Engineering, National Chiao Tung University, Taiwan, Tel: 886-3-573 1830, fax: 886-3-572 4361 email: schung@cc.nctu.edu.tw. **Special discounts apply**.

IEEE EDS Independent Short Courses Registration

Last Name: _____First Name: _____MI:_____

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Newly registered IEEE EDS members may use their Temp ID if they have not yet received their permanent number.
Cost for US members is $113.00 (Basic) + $5.00 Electron Devices Society membership.

To join IEEE EDS go to www.ieee.org/membership/

VANGUARD SERIES

Short Course (please circle):

Dielectrics
April 12, 2001
Santa Clara Marriott, CA

Dielectrics
April 26, 2001
National Chiao Tung Univ.,Taiwan*

Fee for Short Course:

$495 IEEE Member $250 IEEE Student Member $595 Non IEEE Member Total Due:$_____

Fee includes entrance to one short course, one copy of the course notebook, course lunch and two breaks.

Payment may be made by check or credit card.

Must be received no later than 10 days before the short course or a late fee of $25 will be added. A $25 processing fee will be withheld from all refunds.

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*TAIWAN COURSE

To attend the course in Taiwan, please contact IEEE EDS Taipei Chapter Chair Prof. Steve S. Chung, He can be reached at:

Department of Electronics Engineering
National Chiao Tung University
Hsinchu 300, Taiwan
Tel: 886-3-573 1830 fax: 886-3-572 4361
email: schung@cc.nctu.edu.tw

Special discounts apply to this short course.

For office use only: Check#_____Amount $_____ Deposit Date_____
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NEW! from the Electron Devices Society

Vanguard Series short courses will be available SOON on the web and in videotape.

In 2Q 2001, the Electron Devices plans on rolling out short courses that will be delivered to you via the Web or videotapes - your choice! These short courses are based on the live courses already delivered, such as Overview of Fiber Optics and Circuit Designs and Technology for RF-CMOS.

If you missed any of the Vanguard Series short courses last year, here's an opportunity to catch up on these advanced technologies.

For more information, email Emily Sopensky at e.sopensky@ieee.org or call tollfree 877-566-4333 (512 451 4333).

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