Using Modeling to Resolve Design and Reliability Issues

Date
October 19, 2000

Location
The Commons, JJ Pickle Research Center, University of Texas
Austin, Texas

Instructor
Dr. Sanjay Banerjee
Professor, Department of Electrical and Computer Engineering
Director, Microelectronics Research Center
University of Texas at Austin

Topics (tentative)
- Semiconductor physics and p-n junction models
- MOS capacitance-voltage modeling
- MOSFET current-voltage behavior: SPICE type circuit models
- MOSFET short channel effects: DIBL, GIDL, charge sharing, velocity overshoot, quantum-mechanical models
- Bipolar junction transistor models: Hybrid-pi, Ebers-Moll and Gummel-Poon
- BJT second order effects: Early, Kirk, Webster, break down, HBTs
- Reliability Issues in Si ICs: Hot carriers, latchup, gate oxide integrity, electromigration, electrostatic discharge

Course Objectives
- Provide a review about the basics of semiconductor devices and physics
- Discuss the latest MOS and bipolar device compact models
- Provide overview of novel device structures and silicon IC reliability issues

Course Description
This course will provide an overview of MOS and bipolar devices, circuit models and reliability physics. The course will describe the operation and design issues of Si integrated circuits, point out applications and discuss the process integration, reliability and testing issues.

Who Should Attend?
The IEEE Electron Devices Society's independent short courses are intended for experienced electrical and electronic engineers who need quick, intense concentrated information on the latest technologies, and who already have a practical understanding of their own fields of expertise.

The course is especially intended for engineers interested in Si IC design, testing and processing.

About the Instructor


Director of the Microelectronics Research Center and Professor of Electrical and Computer Engineering at the University of Texas at Austin, Dr. Sanjay Banerjee is a renowned expert in ultra-high vacuum and remote plasma-enhanced chemical vapor deposition for silicon-germanium-carbon heterostructure MOSFETs and nanostructures. Banerjee is also interested in the areas of ultra-shallow junction technology and semiconductor device modeling. Banerjee researches fabrication and modeling of high speed, high performance silicon-germanium-carbon-based transistors with the goal of enhancing the electrical charge transported through these devices. The work involves an inter-play between experiments, and theory based on quantum mechanics and solid-state physics. His work has potential applications in high-speed microprocessors, and receives support from industry, the Department of Defense, and the National Science Foundation. In the past he has worked on polysilicon transistors and the first 4-megabit dynamic random access memory.

As a member of the technical staff, Corporate Research, Development and Engineering of Texas Instruments from 1983 to 1987, Banerjee worked on polysilicon transistors, and the physics of the Trench Transistor Cell that was used by Texas Instruments in the world's first 4Megabit DRAM. For this work, he was a co-recipient of the Best Paper Award at the IEEE International Solid State Circuits Conference in 1986.

Banerjee received his M.S. and doctorate from the University of Illinois at Urbana-Champaign in 1981 and 1983, respectively, and his B.Tech from the Indian Institute of Technology, Kharagpur in 1979, all in electrical engineering. He holds the Cullen Trust Endowed Professorship in Engineering No.1 as well as being a Fellow of the Cockrell Family Regents Chair.

A 1996 IEEE Fellow, Banerjee's honors include the IEEE Millennium Medal 2000, Distinguished Lecturer for the IEEE Electron Devices Society (1997-), NSF Presidential Young Investigator Award, 1988 and the Engineering Foundation Advisory Council Halliburton Award, 1991.